REMARKS

Claims 1-7, and 14 – 26 remain in the application. Claims 14-26 are newly added, but do not add any new matter.

The present invention allows improves an overall efficiency of an LED chip. It accomplishes this by allowing more LEDs to be packed into the chip using dividing grooves and bridging wires. The present invention can also allow more than 99% of light emitted towards a substrate from the light emitting layer to be reflected improving an amount of total light emitted by the LEDs by reducing an amount of phosphorus that is on the reflective layer and also by using a Bragg reflecting layer as the reflective layer. (Pg. 14, lns. 19 – 23) Furthermore, the present invention also allows the white light emitted by the LEDs to have a higher or lower color temperature by adjusting a phosphor layer thickness or a percentage of phosphor in the phosphor layer. (Pg. 18, ln. 25 – Pg. 19, ln. 3)

The Office Action rejected Claims 1-13 under 35 U.S.C. § 102 as being anticipated by *Durocher et al.* (U.S. Pat. Pub. No. 2003/0160256).

> [T]he dispositive question regarding anticipation is whether one skilled in the art would reasonably understand or infer from the prior art reference's teaching that every claim [limitation] was disclosed in that single reference.

Dayco Prods., Inc. v. Total Containment, Inc., F.3d 1358, 1368 (Fed. Cir. 2003).

Durocher is directed towards a flexible circuit module by forming a rigid carrier with an LED chip on top of a flexible base. This allows the flexible circuit module to be bent into various shapes so that the flexible circuit can easily fit into a variety of lighting products. (Abstract).

Durocher does not teach or suggest "the plurality of light emitting elements are

connected in series such that a cathode electrode of a light emitting element is connected to an anode electrode of a different light emitting element using a wire formed by a thin metal film formed on the insulating film." As seen in FIG. 8, lead wires 63 are connected to electrodes 37 and bonding pads 61. The electrodes 37 are connected to interconnect patterns 47 and 49. However, *Durocher* does not disclose that an anode electrode from one LED chip 59 is connected to a cathode electrode of another LED chip 59. As seen in FIG. 8, the interconnects 47 and 49 for each LED chip 59 to not touch the interconnects 47 and 49 for another LED chip 59. While *Durocher* indicates that the "LED chips 59 are electrically connected with the interconnected pattern 47, 49 through the electrodes 37 and the lead wires 63" there is no indication that the anode electrode of one LED chip is connected to a cathode electrode of another LED chip. (¶ 0060)

Furthermore, lead wire 63 appears to be in direct contact with only the LED chip 59, bonding pad 61, electrode 37, and encapsulating material 65 as shown in FIG. 10. The encapsulating material 65 can be an epoxy, a glass filed epoxy, a polymer material such as silicone, or phosphorous. Thus, lead wire 63 is not "formed on the insulating film" as recited in Claim 1 of the present invention. Durocher discloses the use of an insulating thermosetting epoxy, but such insulating thermosetting epoxy is only arranged between the heat sink 38 and the LED chips 59 to provide a thermal conduit. (¶ 0058) The heat sink 38, however, does not contact the lead wire 63 and any such insulating thermosetting epoxy material will not contact the lead wire 63.

With respect to Claim 2, *Durocher* also does not disclose "the semiconductor multilayer structure includes a light reflective layer between the light emitting layer and the one of the plurality of main surface of the substrate." The Office Action on Page 3 cites to base 41 as the

substrate. As seen in FIG. 6 and FIG. 7, reflective metal coating 57 is formed on the side walls 36 and 39 of cavities 35. However, reflective metal coating 57 is not located between LED chip59 and base 41. Instead, reflective metal coating 57 is located at about a same height of LED chip 59 in a lateral direction from LED chip 59.

In contrast, in the present invention, a distributed Bragg reflector ("DBR") layer 10 is located between SiC substrate 4 and light emitting layer 14. (Pg. 11, lns. 11 – 29, Pg. 14, lns. 19 - 24; FIG. 4A) The DBR layer 10 positioned in this manner reflects more than 99% of blue light emitted from the light emitting layer 14 towards the SIC substrate 4 back toward the light extraction surface. (Pg. 14, lns. 19 – 24)

With respect to Claim 5, *Durocher* does not disclose that "at least a part of each of the first conductive member and the second conductive member is a plated-through hole provided in the substrate." *Durocher* disclose the use of interconnect patterns 49 in via holes 51, but Durocher does not disclose what the interconnect patterns are. (¶ 0048; FIG. 4) *Durocher* makes no mention that they should specifically be plated-through holes.

In contrast, in the present invention, plated through hole 42 is electrically connected to cathode electrode 32 through bridging wire 40 and also power supply terminal 36. In addition plated through hole 46 is electrically connected via bridging wire 44 to anode electrode 34 and power supply terminal 38. (Pg. 13, ln. 23 – Pg. 14, ln. 6; FIG. 4A, FIG. 4B)

With respect to Claim 6, Durocher fails to teach or suggest "wherein each of the plated-through holes is located at a different corner of the substrate." FIG. 4 through FIG. 13 In *Durocher* each depict the use of six interconnect patterns 49. However, the middle four interconnect patterns 49 are not located at a corner of the base 41.

In contrast, in the present invention, plated-through holes 42 and 46 are located on

different corners of substrate 4 as seen in FIG. 5C.

With respect to Claim 16, *Durocher* also does not teach or suggest "wherein the semiconductor multilayer structure has a structure of epitaxial growth on the substrate." There is no indication in *Durocher* that LED chip 59, or carrier 31 have a structure of epitaxial growth.

In contrast, in the present invention, the LEDs 6 are formed on a main surface of the SiC substrate 4 by epitaxial growth. (Pg. 10, ln. 17 – 19).

With respect to Claim 18, *Durocher* fails to recite "wherein the anode electrode for each of the plurality of light emitting elements includes a transparent electrode." Durocher makes no mention that the electrodes 37 should be transparent. This is due to the fact that the electrodes are below the LED chip 59 as seen in FIG. 7.

In contrast, in the present invention, the anode electrode for LED 6 is formed by the Ni/Au thin film 20 and the ITO transparent electrode 22 to improve transmission of the light emitted from the light emitting layer 14. (Pg. 12, lns. 5 – 12)

With respect to Claim 19, Durocher also does not teach or suggest "wherein the light reflective layer is a distributed Bragg reflector layer." Durocher discloses that the reflective metal coating 57 may comprise sputter and photolithographically patterned aluminum, but does not indicate that it should be a distributed Bragg reflector layer. (¶ 0051)

In contrast, the light reflective layer in the present invention can be a distributed Bragg reflector layer 10 including 30 periods of n-ALGaN/GaN, and n-GaN clas layer 12. (PG. 11, lns. 23 – 16)

With respect to Claim 24, *Durocher* fails to disclose the steps of "dividing the semiconductor multilayer structure into a plurality of portions each of which corresponds to a semiconductor light emitting device" and "dividing the substrate for each of the plurality of

portions of the semiconductor multilayer structure." *Durocher* teaches in FIG. 3 the use of a rigid carrier 31. As seen in FIG. 3, rigid carrier 31 is divided into a plurality of cavities 35. However, rigid carrier 31 does not include an LED chip 59 already. Instead, LED chip 59 must be added at a later time period as shown in FIG. 7. Furthermore, as seen in FIG. 3, FIG. 4, and FIG. 7, the substrate is not divided to separate each LED chip 59 from each other and instead, the cavities 35 are separated by side 32. Even in FIG. 13, where side 32 is absent, an adhesive layer 53 or 55 is still present.

In contrast, in the present invention as illustrated in step A1 in FIG. 6, a lamination layer of the semiconductor multilayer structure including n-AlGaN buffer layer 108, a DBR layer 110 composed of 30 periods of n-AlGaN/GaN, an n-GaN clad layer 112, an InGaN/GaN MQW light emitting layer 114, a p-GaN clad layer 116 and a p-GaN contact layer 118 is formed on a non-doped SiC substrate 104. (Pg. 15, lns. 11 – 17) An unmasked area of the lamination area is etched to divide the lamination layer into portions which correspond to each of the LEDs 6. (Pg. 15, ln.s 19 – 27) As seen in FIG. 6, the lamination layer includes a light emitting layer 114. Furthermore, in step C1, division grooves 26 are formed exposing the SiC substrate 104. (Pg. 16, lns. 2 – 10)

With respect to Claim 25, *Durocher* does not disclose "varying a percentage of phosphor in the phosphor film to vary a color temperature of a white light emitted by the semiconductor light emitting device." *Durocher* disclose that various phosphors and LEDs may be used to achieve an output that appears white or another desired color, but does not disclose that an amount of phosphor can be varied instead of varying a type of phosphor to achieve differences in color temperature. *Durocher* also makes no mention of adjusting the color temperature.

Likewise, with respect to Claim 26, Durocher fails to disclose "varying a thickness of the

phosphor film to vary a color temperature of a white light emitted by the semiconductor light emitting device." Again, *Durocher* does not indicate that the thickness of the phosphor film can be varied to adjust the color temperature or that the thickness of the phosphor film should be varied to include such an adjustment to the color temperature.

In contrast, in the present invention, the color of white light emitted from the LED array chip 2 is determined by a ratio between blue light from the light emitting layer 14 and yellow light from the phosphor 48. This ratio can be adjusted by changing the percentage of the phosphor particles included in the silicone resin and the thickness of the phosphor film 48. When the percent of phosphor particles is higher, or the thickness of the phosphor film 48 is larger, the ratio of yellow light becomes higher. A higher ratio of yellow light results in the white light having a low color temperature. (Pg. 18, ln. 22 – Pg. 19, ln. 6)

All arguments for patentability with respect to Claim 1 are repeated and incorporated herein for Claims 20, 22, and 23.

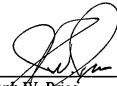
Dependent Claims 2-7, 14-19, 21, and 25-26 depend from and further define Claims 1, 20, and 24 and are thus allowable, too.

It is now believed the present application is in condition for allowance and an early notification of the same is requested.

If there are any questions with regards to this matter the undersigned attorney can be contacted at the below listed telephone number.

Very truly yours,

SNELL & WILMER L.L.P.



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